Hardware Abstraction Layer for non-OpenFlow capable devices

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Abstract

This paper describes a way forward for adding SDN-based control on network devices that are not compatible with OpenFlow. OpenFlow is now considered a leading protocol for future production network control, yet not all domains come with compatible supporting frameworks. We introduce a Hardware Abstraction Layer (HAL) for non-OpenFlow capable devices that addresses this problem and discuss its advantages. In particular, we explain how a HAL-based architecture can support different classes of network devices.

Introduction

Software Defined Networking (SDN) [1] capitalizes on splitting the data and control planes and offers researchers new opportunities for network control and management. Without going into full details in this extended abstract, a controller that sits in the Network Operation System layer is capable of taking global decisions about the data plane traffic control. Although the OpenFlow protocol [1] is now widely used for communication between a logical Controller and Network Devices, many network devices do not support it natively, be that due to the nature of the forwarding paradigm or because of legacy reasons. OpenFlow was designed for wired Ethernet and does not support, e.g., circuit-switched and wireless platforms. The Hardware Abstraction Layer (HAL) [2,3], defined and developed within the FP7 ALIEN [2] project, is an experimentally-verified concept for describing network device capabilities and controlling the forwarding behavior of all OpenFlow and non-OpenFlow capable hardware throughout a network.

Abstraction layers are well known tools in operating systems development that allow direct access to the hardware through drivers which hide hardware complexity and implement platform-specific details. In operating systems such as Linux and Android, unified and standardized sets of routines allow one to write architecture-independent and portable applications. Similarly, in the SDN domain, HAL hides the hardware complexity as well as technology and vendor-specific features, thus presenting a unified abstraction layer for an OpenFlow controller.

Hardware Abstraction Layer: Architecture

HAL follows a modular architecture with unified interfaces for different types of the network equipment. The main assumptions for the HAL architecture [2,3] are:

- HAL resides between the OpenFlow Controller and the non-OpenFlow network device i.e. OpenFlow Controller can get the control access on data path only through the HAL.
- HAL components are reusable. HAL layer is divided into two parts, i.e. hardware dependent and independent sub-layers. This approach is similar to the Java concept, where the platform dependent (JVM) and platform independent (java class files) parts have been identified. This approach leads to smaller code, better troubleshooting and software management.
- HAL is portable, giving an opportunity to implement OpenFlow on various, currently non-OpenFlow-enabled platforms.

As depicted on Figure 1, HAL comprises two parts: Hardware Agnostic Part (HAP) and Hardware Specific Part (HSP). HAP enables build-in virtualization and OpenFlow communication mechanisms that are independent of the underlying hardware platform. HSP is a set of hardware drivers realizing atomic network instructions, specific to different hardware platforms.

OpenFlow protocol routines are transferred through HAL to hardware-specific commands and configurations via a Translator module. Drivers, which have direct access to the Network Device, configure the device through available programming interfaces, platform-specific APIs, or other pre-existing configuration and management interfaces in the case of “closed” hardware. HAL can configure also a set of devices in systems composed with multiple network elements (e.g., GEPON or DOCSIS systems) in which a single device cannot be configured individually. In case of such systems, the Orchestrator module enables the distribution of the configuration instructions to each network device.

A virtualization component is also foreseen within the architecture to provide virtualization capabilities to HAL-compatible devices. By interacting with the Network Management System (NMS) to properly configure the virtual network instances, this component enables a flowspace slicing among many controllers managing several virtual node instances using different versions of the OpenFlow protocol.

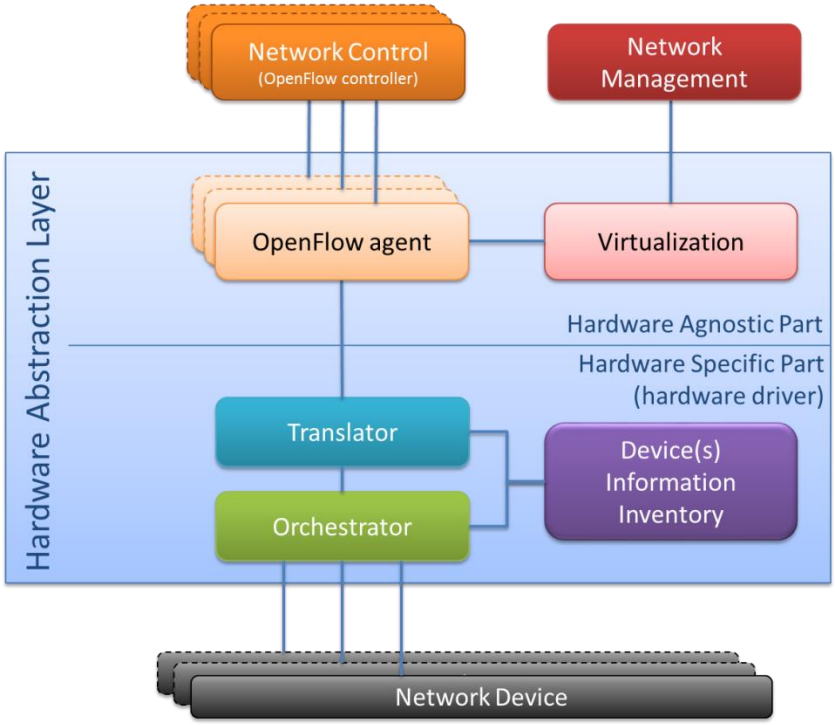

Figure 1 Hardware Abstraction Layer: Architecture

The initial HAL architecture has been described in [3], the publicly available publication released by the ALIEN Consortium. The HAL implementation follows naturally from this model. Modular software design allows the separation of the evolution of the OpenFlow management endpoint (a common part for all hardware platforms) and hardware specific drivers which communicate with the network equipment. The HAL architecture makes the implementation of OpenFlow protocol easier for any new device that is "alien" for this technology.

Hardware Abstraction Layer: Implementation

Based on the above-mentioned dual-layered concept, HAL is actively implemented and tested in the FP7 ALIEN project based on ROFL [4] and xDPd [5]. The hardware agnostic and hardware specific sub-layers of HAL are merged through the Abstract Forwarding API (AFA) [4,5] interface which is common for different hardware platforms. AFA binds the platform-specific forwarding module with the control and management modules of xDPd. This implementation framework based on xDPd/ROFL/AFA is subsequently mapped to the HAL architecture, as illustrated in Figure 2.

ROFL implements various versions of the OpenFlow protocol (OF1.0, OF1.2 and OF1.3) [1] as well as a definition of the AFA internal interface. xDPd is a framework for HAL instantiation in a form of one or

many OpenFlow endpoints (OpenFlow agents). Each OpenFlow endpoint is associated with one hardware driver for a given hardware platform.

On some hardware platforms (e.g., containing an open-access network processor), the common software implementation of the OpenFlow pipeline can be deployed and then the network device acts a hardware accelerator for network packet processing. Acceleration is enabled by the Pipeline Hardware API [4,5], i.e. an abstract representation of network packets processed by the hardware.

In the ALIEN project, HAL implementation is validated on several network equipment platforms such as EZappliance with EZchip NP3 network processor, GEPON, NetFPGA, DOCSIS, ATCA with Cavium Octeon network processor, ADVA Layer 0 Switch, Dell/Force10 7024 switch with ASIC and Cavium Octeon. At the time of this writing, the xDPd forwarding module has been already implemented and tested on several platforms, including OCTEON, Broadcom and GNU/Linux. All these implementations are publicly available [4,5].

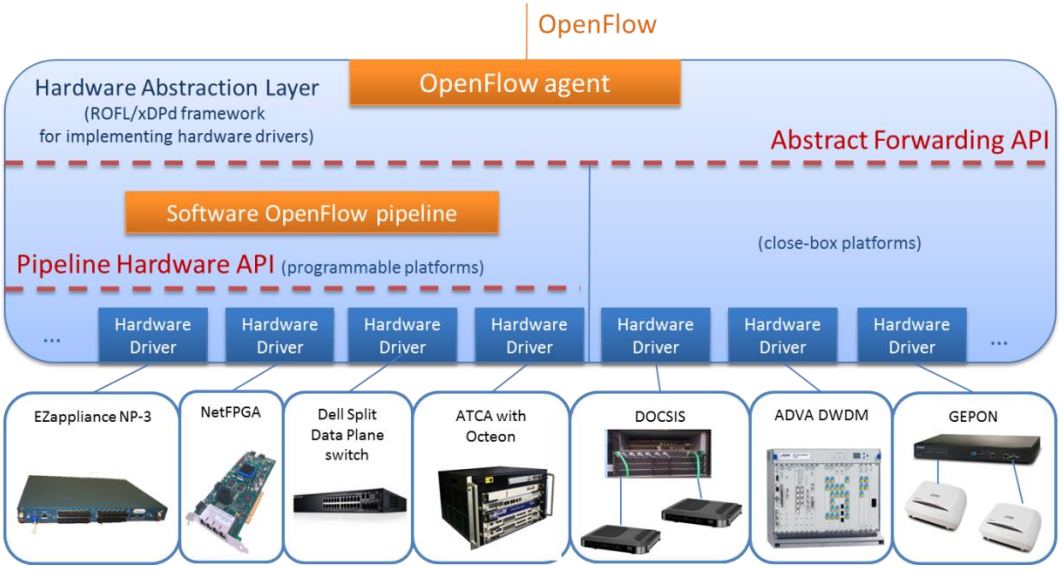

Figure 2 Hardware Abstraction Layer: Implementation

HAL Design Considerations and Advantages

The OpenFlow protocol itself is an abstraction layer for network devices, but its implementation is still a quite complex task. This makes SDN implementation based on OpenFlow a really coarse-grained system, far behind the level of granularity observed in operating systems. The pace of development in these two areas is also still incomparable despite the tremendous advances which have already been made thanks to OpenFlow.

The ALIEN HAL architecture adds an abstraction layer inside an OpenFlow implementation. This solution is addressed to network equipment vendors. The separation of hardware-related parts such as forwarding chip configuration, and general parts such as the OpenFlow protocol endpoint, enable extensive code reuse in various use cases. OpenFlow protocol implementation for a new device (or a new version of an existing device) will require only an adaptation of the HSP code. Implementation of

new versions of the OpenFlow protocol will be faster as well. Such operation will require only a new HAP that will be reused without modifications on all devices produced by a given vendor.

Summary and Future Work

The main objective of the FP7 ALIEN project is to define the Hardware Abstraction Layer (HAL) enabling non-OpenFlow capable hardware to be controlled through the OpenFlow protocol in a consistent manner. This abstraction layer is the key enabler towards enhanced network programmability on a diverse set of devices that do not adhere to the Ethernet model upon which the original OpenFlow work is based. The HAL architecture presented in this paper, as well as its implementation, may be reused by hardware vendors and developers when implementing OpenFlow on these hardware platforms that do not support it natively.

By September 2014, the work described in this paper will be integrated with the OFELIA Control Framework [6] and tested with the CCN application developed by CONET [7]. We aim to present a demo of the HAL implementation at TNC 2014, should this paper be accepted.

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Author Biographies

Łukasz Ogrodowczyk received the M.Sc. in the Electronics and Telecommunications, majoring in the Networks of Information Transport, from the Poznan University of Technology in 2007. From 2010 he works in Poznan Supercomputing and Networking Center. Co-author of some papers for international conferences (e.g. CSNDSP2012, Networks2012, Terena2013). He was involved in the polish project Future Internet Engineering. Currently he works in the international project ALIEN. Łukasz is familiar with embedded systems, some programming languages like C and Python, network protocols and Quality of Service in next generation packet networks.

Bartosz Belter received the M.Sc. degree in Computer Science from the Poznan University of Technology in 2002. He works in Poznan Supercomputing and Networking Center as a Senior Network Engineer. He participated in several FP6 IST projects: 6NET (IST-2001-32063), PHOSPHORUS (IST034115) and GN2 (IST511082). He also participated in a number of national initiatives funded by Polish Ministry of Science and Higher Education (Clusterix, Polish LDAP and others). Currently he is involved in several EU funded projects. His main research activities concern the architectural aspects of Control and Management Planes in optical networks and Quality of Service in next generation packet networks. He is author or co-author of papers in professional journals and conference proceedings.

Artur Binczewski received the M.Sc. degree in Computer Science from the Poznan University of Technology in 1993. He is the Manager of Network Division at the PSNC. He was involved in several EC projects: SEQUIN (IST-1999-20841), ATRIUM (IST-1999-20675), 6NET (IST-2001-32063). He coordinated the Porta Optica Study (RI026617), PHOSPHORUS (IST034115), ADDONAS (PIANO+) and ALIEN (317880) projects. He is author or co-author of papers in major professional journals and conference proceedings.

Krzysztof Dombek received the M.Sc. degree in 2008 from the University of Technology and Life Sciences in Bydgoszcz, Poland. He's a Computer System Analyst in Polish NREN – Poznan Supercomputing and Networking Center. He was a participant of many European research projects e.g. PHOSPHORUS, GEANT3 or GEYSERS. He was also involved in national project of the Future Internet Engineering. At present he's a participant of ALIEN project founded by EU in FP7 where he's involved in integration with the OFELIA Control Framework.

Artur Juszczyk received the M.Sc. degree in the Electrical Engineering, majoring in the Microprocessors and Control Systems, at the Poznan University of Technology in 2005. He works in the Poznan Supercomputing and Networking Center since 2007 as a computer systems analyst. He took part in the several European and national projects, PHOSPHORUS, GEYSERS, GEANT and Future Internet Engineering as a programmer, tester, system engineer. He is currently involved in the international project ALIEN. His interests focus on the Unix base systems, virtualization of resources, management of network infrastructure and next-generation networks.

Iwo Olszewski received the M.Sc. degree in Computer Science, majoring in the Computer Networks and Distributed Systems, from the Poznan University of Technology in 2010. He started working in PSNC in 2006 as an network operator in PIONIER NOC. In 2010 he has joined the NGN Team as an analyst/developer. He has experience in object-oriented programming in Java and C# and deep knowledge about network protocols and devices. He is familiar with EZchip network processors and Juniper Junos platform development. He was involved in the national project Future Internet Engineering and FP7 project NOVI. Currently he devotes his time to the ALIEN project. Co-author of several papers in conference proceedings (CSNDSP, NETWORKS, SNPD, TNC).

Damian Parniewicz received the M.Sc. degree in Telecommunication from the Poznań University of Technology (2005) and currently is a network systems analyst in Poznan Supercomputing and Networking Center. He has participated in several European Union Research and Development projects related to network management, optical network equipment and control planes (FP6 and FP7 IST projects: MUPBET, PHOSPHORUS, GEANT3, GEYSERS, ALIEN and Polish national project: Future Internet Engineering). His major interest areas are control planes protocols for networks and VoIP systems, traffic engineering and software technologies.

Roberto Doriguzzi Corin received his degree in Mathematics in 1996 from the University of Trento, Italy, with a thesis in calculus of variations. From 1999 to 2008 he was employed in Neuricam S.p.A. in Trento as Linux embedded systems programmer, network system administrator and head of the software development team. In year 2008 he joined CREATE-NET where he is currently working as Research Engineer and is leading the "Network Virtualization & Embedded systems" group. His main research interests are software-defined networking, network virtualization and embedded systems.

Matteo Gerola received his Master degree on Telecommunications Engineering in 2007 from the University of Trento. From October 2005 to July 2006 he has been working on WiMAX experimentation in CSP, an innovation and research centre based in Turin. He joined CREATE-NET in July 2007 where he is currently working as Research Engineer. He is now on an internship at ON.Lab, the no-profit research lab founded by SDN inventors and leaders from Stanford University and UC Berkeley whose aim is to foster an open source community to develop SDN tools and platforms. His main research interests are network virtualization and software-defined networking.

Dr. Elio Salvadori is a Senior Research Advisor in CREATE-NET. He graduated in Telecommunications Engineering at Politecnico di Milano in 1997. He worked as systems engineer in Nokia Networks and then Lucent Technologies until November 2001, when he moved to the University of Trento where he got his Ph.D. degree in ICT in 2005. He then joined CREATE-NET in 2005, where he's been acting as Head of the "Engineering and Fast Prototyping" Area since 2008. Beside a strong involvement on control plane technologies for optical networks, his team has been working on OpenFlow and SDN technologies since 2010. He has been lately involved in the rollout of a large FTTH network in Trentino (Italy). He authored a number of publications in the area of optical networks and software-defined networking.

Kostas Pentikousis is the Head of IT Infrastructure at EICT GmbH, Berlin, Germany. He earned his Bachelor's degree in informatics from Aristotle University of Thessaloniki, and his Master's and doctoral degrees in computer science from Stony Brook University.

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Dr. Eduardo Jacob spent 5 years in a public R&D in Telecommunications enterprise and as IT director in the private sector before becoming assistant professor in the Faculty of Engineering of Bilbao (SPAIN) of the University of the Basque Country. He is the leader of the research group project involved in this project (EHU-OEF). He has been project reviewer for the Spanish and Basque government and has participated in the design of the strategic plan for Science, Technology and Society (2005-2008) of the Basque Government. He is also part Advisory Council of the Basque Data Protection Agency and he is member of the UPV/EHU ICT commission. He has participated in several Regional (Basque Country), National and European projects. His current interests are linked to Sofware Defined Networking, Neutral Access Networks over OpenFlow enabled infrastructures.

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